## DECADE COUNTER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs

**L SUFFIX**
CERAMIC
CASE 620

**P SUFFIX**
PLASTIC
CASE 648

**D SUFFIX**
SOIC
CASE 751B

### ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A$ = −55° to 125°C for all packages.

### MAXIMUM RATINGS* (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) | −0.5 to $V_{DD}$ +0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient), per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8-Second Soldering) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

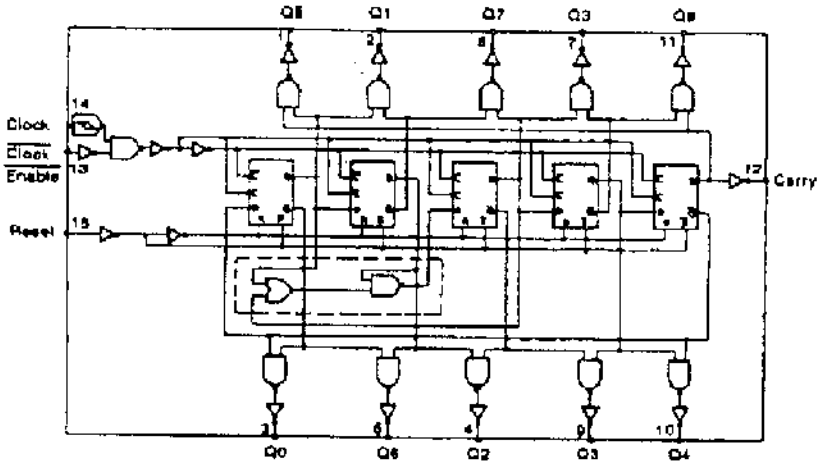
### FUNCTIONAL TRUTH TABLE

(Positive Logic)

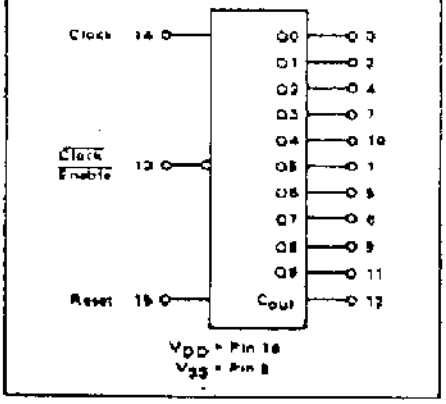
| CLOCK | CLOCK ENABLE | RESET | DECODE OUTPUT |
|---|---|---|---|
| 0 | X | 0 | n |
| X | 1 | 0 | n |
| X | X | 1 | Q0 |
| ⌐ | 0 | 0 | n+1 |
| ⌐ | X | 0 | n |
| X | ⌐ | 0 | n |
| 1 | ⌐ | 0 | n+1 |

X = Don't Care. If n ≤ 5 Carry = "1", Otherwise = "0"

### LOGIC DIAGRAM




### BLOCK DIAGRAM

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**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55°C Min | −55°C Max | 25°C Min | 25°C Typ # | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| "1" Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage "0" Level<br>($V_O$ = 4.5 or 0.5 Vdc) | $V_{IL}$ | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| "1" Level<br>($V_O$ = 0.5 or 4.5 Vdc) | $V_{IH}$ | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current<br>($V_{OH}$ = 2.5 Vdc) Source | $I_{OH}$ | 5.0 | −3.0 | — | −2.4 | −4.2 | — | −1.7 | — | mAdc |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | −0.64 | — | −0.51 | −0.88 | — | −0.36 | — | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | −1.6 | — | −1.3 | −2.25 | — | −0.9 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | −4.2 | — | −3.4 | −8.8 | — | −2.4 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | $I_{in}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | µAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current<br>(Per Package) | $I_{DD}$ | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | µAdc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Total Supply Current**†<br>(Dynamic plus Quiescent, Per Package)<br>($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (0.27 µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 10 | $I_T$ = (0.55 µA/kHz) f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (0.83 µA/kHz) f + $I_{DD}$ | | | | | | | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

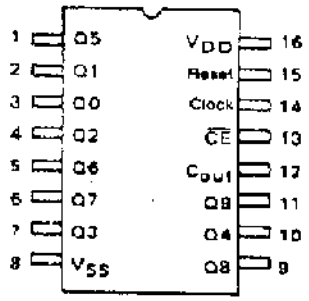
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in µA (per package), $C_L$ in pF, V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.0011.

**PIN ASSIGNMENT**




This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**SWITCHING CHARACTERISTICS*** ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ # | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | | 5.0 | — | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | — | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | — | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| Reset to Decode Output | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 415 ns | | 5.0 | — | 500 | 1000 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 197 ns | | 10 | — | 230 | 460 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 150 ns | | 15 | — | 175 | 350 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| Clock to $C_{out}$ | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 315 ns | | 5.0 | — | 400 | 800 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 142 ns | | 10 | — | 175 | 350 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 100 ns | | 15 | — | 125 | 250 | |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | ns |
| Clock to Decode Output | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 415 ns | | 5.0 | — | 500 | 1000 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 197 ns | | 10 | — | 230 | 460 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 150 ns | | 15 | — | 175 | 350 | |
| Turn-Off Delay Time | $t_{PLH}$ | | | | | ns |
| Reset to $C_{out}$ | | | | | | |
| $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 315 ns | | 5.0 | — | 400 | 800 | |
| $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 142 ns | | 10 | — | 175 | 350 | |
| $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 100 ns | | 15 | — | 125 | 250 | |
| Clock Pulse Width | $t_{w(H)}$ | 5.0 | 250 | 125 | — | ns |
| | | 10 | 100 | 50 | — | |
| | | 15 | 75 | 35 | — | |
| Clock Frequency | $f_{cl}$ | 5.0 | — | 5.0 | 2.0 | MHz |
| | | 10 | — | 12 | 5.0 | |
| | | 15 | — | 16 | 6.7 | |
| Reset Pulse Width | $t_{w(H)}$ | 5.0 | 500 | 250 | — | ns |
| | | 10 | 250 | 125 | — | |
| | | 15 | 190 | 95 | — | |
| Reset Removal Time | $t_{rem}$ | 5.0 | 750 | 375 | — | ns |
| | | 10 | 275 | 135 | — | |
| | | 15 | 210 | 105 | — | |
| Clock Input Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | No Limit | | | — |
| | | 10 | | | | |
| | | 15 | | | | |
| Clock Enable Setup Time | $t_{su}$ | 5.0 | 350 | 175 | — | ns |
| | | 10 | 150 | 75 | — | |
| | | 15 | 115 | 52 | — | |
| Clock Enable Removal Time | $t_{rem}$ | 5.0 | 420 | 260 | — | ns |
| | | 10 | 200 | 100 | — | |
| | | 15 | 140 | 70 | — | |

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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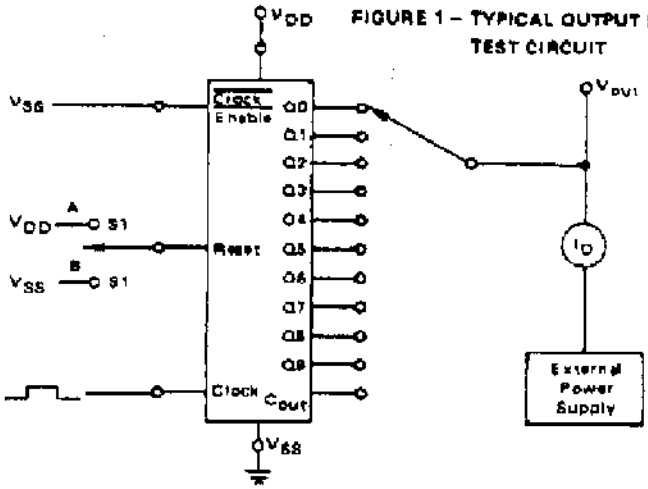
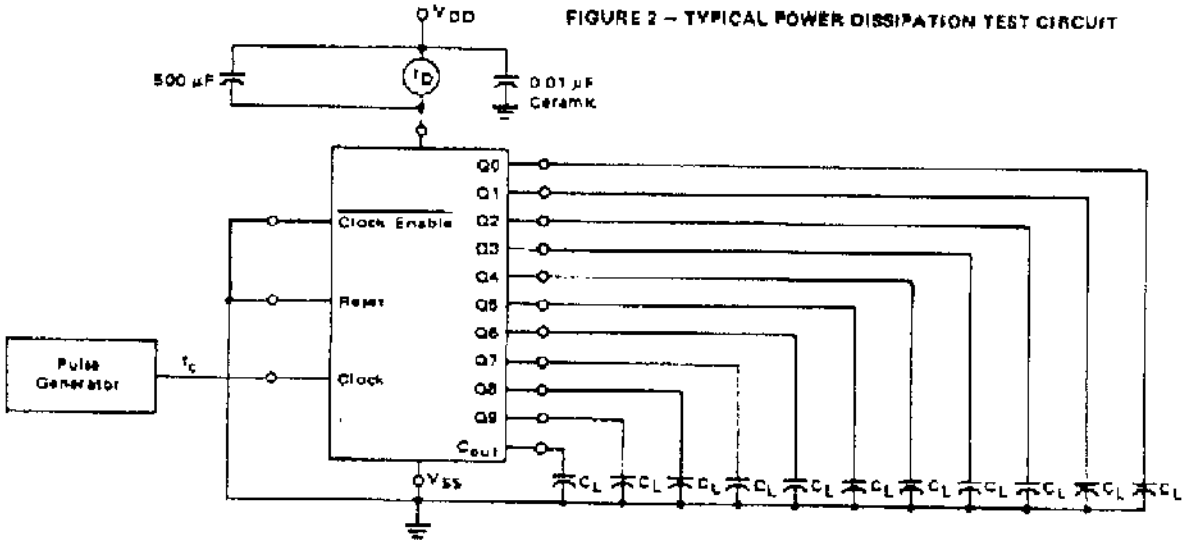
FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT




| | OUTPUT SINK DRIVE | OUTPUT SOURCE DRIVE |
|---|---|---|
| DECODE OUTPUTS | (S1 to A) | Clock to desired outputs (S1 to B) |
| Carry | Clock to 5 thru 9 (S1 to B) | S1 to A |
| $V_{GS}$ * | $V_{DD}$ | $-V_{DD}$ |
| $V_{DS}$ * | $V_{out}$ | $V_{out}-V_{DD}$ |

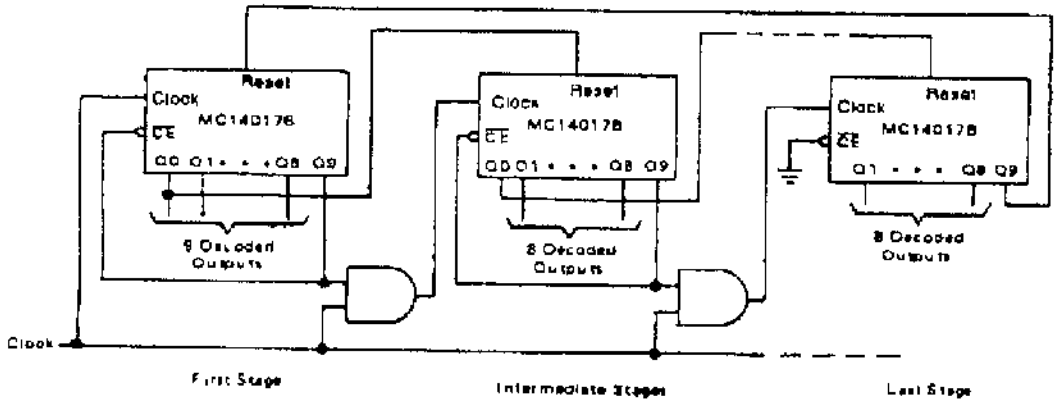
FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

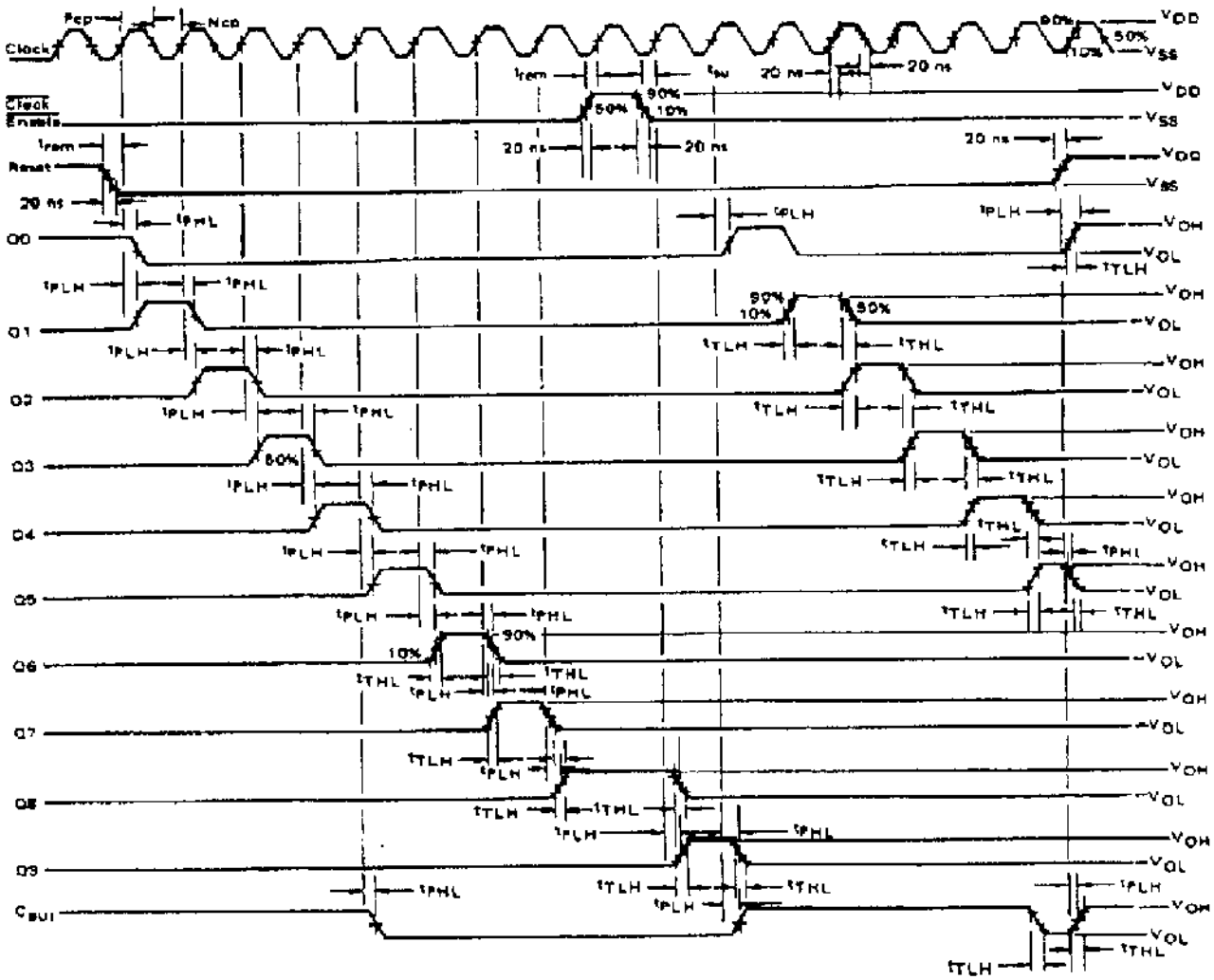



## APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION




Clock
Clock Enable
Reset
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
$C_{out}$
$V_{DD}$
$V_{SS}$
$V_{OH}$
$V_{OL}$
20 ns
50%
90%
10%